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Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1

of 5

Complete if Known

Application Number	10/762,181
Filing Date	January 21, 2004
First Named Inventor	Mohklesi
Art Unit	
Examiner Name	
Attorney Docket Number	SAND-01021US0

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 5,043,940	8/27/1991	Harari	
		US- 5,095,344	3/10/1992	Harari	
		US- 5,172,338	12/15/1992	Mehrotra et al.	
		US- 5,343,063	8/30/1994	Yuan et al.	
		US- 5,570,315	10/29/1996	Tanaka et al.	
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		US- 5,774,397	6/30/1998	Endoh et al.	
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		US- 5,936,887	8/10/1999	Choi et al.	
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		US- 6,121,654	9/19/2000	Likharev	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
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Sheet 3	of 4	Attorney Docket Number	SAND-01021US0

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	1	BORSON, et al., "Direct Measurement of the Energy Distribution of Hot Electrons in Silicon Dioxide," J. Appl. Phys., Vol. 58, No. 3.1, August 1985, pp. 1302-1313	
	2	BROWN, et al., "Nonvolatile Semiconductor Memory Technology, A Comprehensive Guide to Understanding and Using NVSM Devices," IEEE, pp. 198-200	
	3	CAMM, et al., "Engineering Ultra-Shallow Junctions Using rRTP™," IEEE, Vortek Industries Limited, 2002	
	4	CHAN, et al., "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device," IEEE Electron Device Letters, Vol. EDL-8, No. 3, March 1987, pp. 93-95	
	5	CHOI, et al., "A Novel Booster Plate Technology in High Density NAND Flash Memories for Voltage Scaling-Down and Zero Program Disturbance," IEEE Symposium on VLSI Technology Digest of Technical Papers, 1996, pp. 238-239	
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	7	DIJKSTRA, et al., "ISSG RTO (In-situ Steam Generation Rapid Thermal Oxidation) Grown Tunnel Oxide for Improved Reliability of Flash Memories," Philips Semiconductors, pp. 85-86	
	8	DiMARIA, "Graded or Stepped Energy Band-Gap-Insulator MIS Structures (GI-MIS or SI-MIS)," American Institute of Physics, September 1979, pp. 5826-5828	
	9	DiMARIA, et al., "Dual-Electron-Injector-Structure Electrically Alterable Read-Only-Memory Modeling Studies," IEEE Transactions on Electron Devices, Vol. ED-28, No. 9, September 1981, pp. 1047-1053	
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		DIMARIA, et al., "Extended Cyclability in Electrically-Alterable Read-Only-Memories," IEEE ELECTRON DEVICE LETTERS, VOL. EDL-3, NO. 7, July 1982, pp. 191-195	
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		OHMI, et al., "New Paradigm of Silicon Technology," Proceedings of the IEEE, Vol. 89, No. 3, March 2001, pp. 394-412	
		OHTSUBO, et al., "Low Temperature Growth (400°C) of High-Integrity Thin Silicon-Oxynitride Films by Microwave-Excited high-Density Kr/O ₂ /NH ₃ Plasma," pp. 166-169	

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		SATOH, et al., "A Novel Channel Boost Capacitance (CBC) Cell Technology with Low Program Disturbance Suitable for Fast Programming 4Gbit NAND Flash Memories", IEEE Symposium on VLSI Technology Digest of Technical Papers, 1998, pp. 108-109	
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